

Voltage-divider bias

DC theory and resistor-bank tutorials

Purpose. A quiescent point, or Q point, describes the transistor DC condition before an applied signal changes the circuit. The divider sets the base voltage. Subtracting the base-emitter voltage gives the emitter voltage; the emitter resistor then determines the emitter current.

Circuit model. Figure 1 uses R_1 as the upper divider resistor, R_2 as the lower divider resistor, R_C in the collector branch and R_E in the emitter branch.

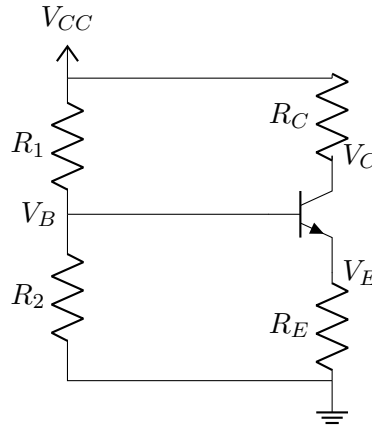


Figure 1: NPN voltage-divider bias circuit.

With base loading neglected and $I_E = I_C$, the governing relations are

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}, \quad V_E = V_B - V_{BE}, \quad (1)$$

$$I_C \approx I_E = \frac{V_E}{R_E}, \quad V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0, \quad (2)$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}, \quad R_C + R_E = \frac{V_{CC} - V_{CEQ}}{I_{CQ}}. \quad (3)$$

Base current loads the divider: $I_{R1} = I_{R2} + I_B$, lowering V_B from the unloaded value. Neglecting that change does not imply zero physical base current. KVL means Kirchhoff's voltage law around the collector-emitter loop [1].

Figure 2 defines the Q point and symbolic load line. The Q point gives the DC condition before an applied signal.

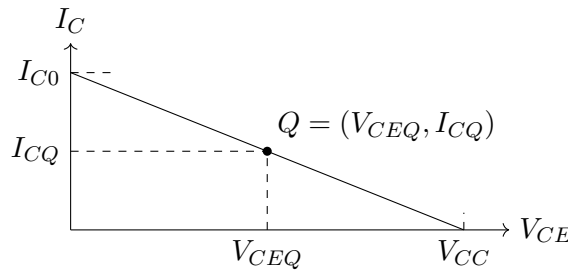


Figure 2: Symbolic collector load line and Q point, not to scale.

Reference [1]. Australian National University, "DC Bias," ENGN2211 course notes. Online source, accessed 8 October 2026.

Complete the three questions and compare calculations within your group. Table 1 supplies the final resistor values for Tutorial 1. Derive the answers for Tutorials 2 and 3 yourselves. No worked solutions are provided. Thursday is Open Day; no in-person lecture will take place.

Tutorial 1: Resistor-bank selection A (5 marks)

Figure 3 shows the required operating point and load line. The design data are specified here.

Supply: $V_{CC} = 12\text{ V}$
 Target collector current: $I_{CQ} = 1\text{ mA}$
 Target collector-emitter voltage: $V_{CEQ} = 6\text{ V}$

Available resistor bank:

20 k Ω , 4 k Ω , 4.7 k Ω , 1.3 k Ω , 10 k Ω , 6.8 k Ω

Use $V_{BE} = 0.70\text{ V}$, $I_E = I_C$ and negligible base loading. Use one resistor for each position. Do not use series combinations, parallel combinations or resistor reuse.

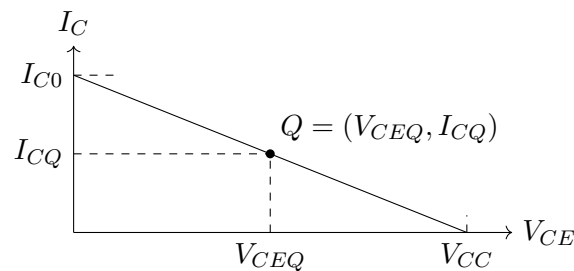


Figure 3: Load line and required Q point; the sketch is not to scale.

- Draw the voltage-divider bias circuit with the four resistor labels R_1 , R_2 , R_C and R_E . Leave numerical values and other labels off the circuit. [1 mark]
- Select four resistors from the bank and show calculations for the four circuit positions. Confirm the target Q point with the divider relation and collector-emitter KVL. [4 marks]

Record every selected value with units in Table 1.

Table 1: Selected resistor values for Tutorial 1.

Position	R_C	R_E	R_1	R_2
Selected value	4.7 k Ω	1.3 k Ω	20 k Ω	4 k Ω

Tutorial 2: Resistor-bank selection B (5 marks)

Figure 4 shows the required operating point and load line. The design data are specified here.

Supply: $V_{CC} = 9\text{ V}$
 Target collector current: $I_{CQ} = 1\text{ mA}$
 Target collector-emitter voltage: $V_{CEQ} = 4\text{ V}$

Available resistor bank:

10 k Ω , 5 k Ω , 2.3 k Ω , 2.7 k Ω , 1 k Ω , 4.7 k Ω

Use $V_{BE} = 0.70\text{ V}$, $I_E = I_C$ and negligible base loading. Use one resistor for each position. Do not use series combinations, parallel combinations or resistor reuse.

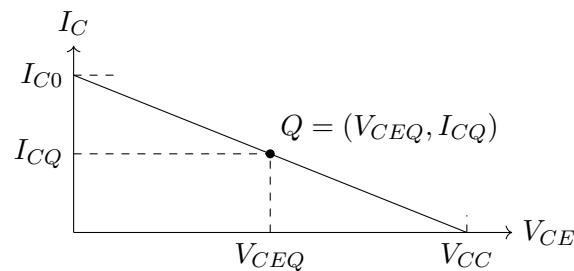


Figure 4: Load line and required Q point; the sketch is not to scale.

- Draw the voltage-divider bias circuit with the four resistor labels R_1 , R_2 , R_C and R_E . Leave numerical values and other labels off the circuit. [1 mark]
- Select four resistors from the bank and show calculations for the four circuit positions. Confirm the target Q point with the divider relation and collector-emitter KVL. [4 marks]

Record every selected value with units in Table 2.

Table 2: Selected resistor values for Tutorial 2.

Position	R_C	R_E	R_1	R_2
Selected value				

Tutorial 3: Resistor-bank selection C (5 marks)

Figure 5 shows the required operating point and load line. The design data are specified here.

Supply: $V_{CC} = 18\text{ V}$
 Target collector current: $I_{CQ} = 1\text{ mA}$
 Target collector-emitter voltage: $V_{CEQ} = 8.9\text{ V}$

Available resistor bank:

50 k Ω , 10 k Ω , 2.3 k Ω , 6.8 k Ω , 4.7 k Ω , 20 k Ω

Use $V_{BE} = 0.70\text{ V}$, $I_E = I_C$ and negligible base loading. Use one resistor for each position. Do not use series combinations, parallel combinations or resistor reuse.

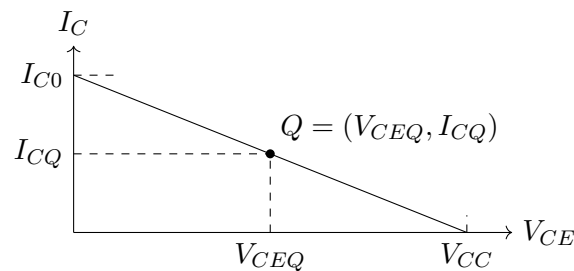


Figure 5: Load line and required Q point; the sketch is not to scale.

- Draw the voltage-divider bias circuit with the four resistor labels R_1 , R_2 , R_C and R_E . Leave numerical values and other labels off the circuit. [1 mark]
- Select four resistors from the bank and show calculations for the four circuit positions. Confirm the target Q point with the divider relation and collector-emitter KVL. [4 marks]

Record every selected value with units in Table 3.

Table 3: Selected resistor values for Tutorial 3.

Position	R_C	R_E	R_1	R_2
Selected value				